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Heterogeneous Reconfigurable Processors for Real-Time Baseband Processing

From Algorithm to Architecture

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Heterogeneous Reconfigurable Processors for Real-Time Baseband Processing Chenxin Zhang,Liang Liu,Viktor Öwall,2016-01-18 This book focuses on domain specific heterogeneous reconfigurable architectures demonstrating for readers a computing platform which is flexible enough to support multiple standards multiple modes and multiple algorithms The content is multi disciplinary covering areas of wireless communication computing architecture and circuit design The platform described provides real time processing capability with reasonable implementation cost achieving balanced trade offs among flexibility performance and hardware costs The authors discuss efficient design methods for wireless communication processing platforms from both an algorithm and architecture design perspective Coverage also includes computing platforms for different wireless technologies and standards including MIMO OFDM Massive MIMO DVB WLAN LTE LTE A and 5G   Run-time Adaptation for Reconfigurable Embedded Processors Lars Bauer,Jörg Henkel,2010-12-01 Embedded processors are the heart of embedded systems Reconfigurable embedded processors comprise an extended instruction set that is implemented using a reconfigurable fabric similar to a field programmable gate array FPGA This book presents novel concepts strategies and implementations to increase the run time adaptivity of reconfigurable embedded processors Concepts and techniques are presented in an accessible yet rigorous context A complex realistic H 264 video encoder application with a high demand for adaptivity is presented and used as an example for motivation throughout the book A novel run time system is demonstrated to exploit the potential for adaptivity and particular approaches algorithms are presented to implement it   Proceeding of 2021 International Conference on Wireless Communications, Networking and Applications Zhihong Qian,M.A. Jabbar,Xiaolong Li,2022-07-12 This open access proceedings includes original unpublished peer reviewed research papers from the International Conference on Wireless Communications Networking and Applications WCNA2021 held in Berlin Germany on December 17 19th 2021 The topics covered include but are not limited to wireless communications networking and applications The papers showcased here share the latest findings on methodologies algorithms and applications in communication and network making the book a valuable asset for professors researchers engineers and university students alike This is an open access book   **2000 IEEE International Conference on Acoustics, Speech, and Signal Processing** ,2000   **Handbook of Green Information and Communication Systems** Alagan Anpalagan,Isaac Woungang,Mohammad S. Obaidat,2012-11-20 This book gives a comprehensive guide on the fundamental concepts applications algorithms protocols new trends and challenges and research results in the area of Green Information and Communications Systems It is an invaluable resource giving knowledge on the core and specialized issues in the field making it highly suitable for both the new and experienced researcher in this area Key Features Core research topics of green information and communication systems are covered from a network design perspective giving both theoretical and practical perspectives Provides a unified covering of otherwise disperse selected topics on green computing

information communication and networking Includes a set of downloadable PowerPoint slides and glossary of terms for each chapter A whose who of international contributors Extensive bibliography for enhancing further knowledge Coverage includes Smart grid technologies and communications Spectrum management Cognitive and autonomous radio systems Computing and communication architectures Data centres Distributed networking Cloud computing Next generation wireless communication systems 4G access networking Optical core networks Cooperation transmission Security and privacy Core research topics of green information and communication systems are covered from a network design perspective giving both a theoretical and practical perspective A whose who of international contributors Extensive bibliography for enhancing further knowledge   Architecture of Computing Systems Christian Hochberger,Lars Bauer,Thilo Pionteck,2021-07-14 This book constitutes the proceedings of the 34th International Conference on Architecture of Computing Systems ARCS 2021 held virtually in July 2021 The 12 full papers in this volume were carefully reviewed and selected from 24 submissions 2 workshop papers VEFRE are also included ARCS has always been a conference attracting leading edge research outcomes in Computer Architecture and Operating Systems including a wide spectrum of topics ranging from fully integrated self powered embedded systems up to high performance computing systems It also provides a platform covering newly emerging and cross cutting topics such as autonomous and ubiquitous systems reconfigurable computing and acceleration neural networks and artificial intelligence The selected papers cover a variety of topics from the ARCS core domains including heterogeneous computing memory optimizations and organic computing   *Introduction to Reconfigurable Computing* Christophe Bobda,2007-09-30 Introduction in Reconfigurable Computing provides a comprehensive study of the field Reconfigurable Computing It provides an entry point to the novice willing to move in the research field reconfigurable computing FPGA and system on programmable chip design The book can also be used as teaching reference for a graduate course in computer engineering or as reference to advance electrical and computer engineers It provides a very strong theoretical and practical background to the field of reconfigurable computing from the early Estrin s machine to the very modern architecture like coarse grained reconfigurable device and the embedded logic devices Apart from the introduction and the conclusion the main chapter of the book are the following Architecture of reconfigurable systems which presents the technology and the architecture used in fined grained and those used in coarse grained reconfigurable devices Design and implementation This section deals with the implementation on reconfigurable system It briefly covers the steps needed to implement application on today s FPGAs And focus on the logic synthesis for FPGA in particular LUT technology mapping High Level Synthesis for Reconfigurable Devices The high level synthesis for reconfigurable systems also known as temporal partitioning is presented here Several temporal partitioning techniques are presented and explained Temporal placement This section considers stand alone reconfigurable systems Its assume that a kind of operating systems for reconfigurable systems is in charge of managing the resources of a given system and allocate space on a device for the computation of

incoming tasks and therefore presents several temporal placement approaches for off line as well as on line placement On line and Dynamic Interconnection This chapter reviews andexplains the different approaches for allowing communication between modules dynamically placed at run time on a given device Designing a reconfigurable application on Xilinx Virtex FPGA In this section the different design approaches of partial reconfigurable systems on the Xilinx FPGAs that are one of the few one on the market with this feature is explained System on programmable chip System on programmable chip is a hot topic in reconfigurable computing This is mainly the integration of a system made upon some peripheral UART Ethernet VGA etc but also computational Coding filter etc hardware modules on one programmable chip The current usable solutions are presented The book furthermore focusses on the development of adaptive multiprocessors on chip i e systems consisting of a set of Processors and exchangeable hardware accelerators Applications This part covers the use of reconfigurable system in computer architecture rapid prototyping reconfigurable supercomputer reconfigurable massively parallel computers and algorithm better adapted for reconfigurable systems distributed arithmetic network packet processing etc

Applied Reconfigurable Computing. Architectures, Tools, and Applications Francesca Palumbo,Georgios Keramidas,Nikolaos Voros,Pedro C. Diniz,2023-09-15 This book constitutes the proceedings of the 19th International Symposium on Applied Reconfigurable Computing ARC 2023 which was held in Cottbus Germany in September 2023 The 18 full papers presented in this volume were reviewed and selected from numerous submissions The proceedings also contain 4 short PhD papers The contributions were organized in topical sections as follows Design methods and tools applications architectures special session near and in memory computing and PhD forum papers   A Reconfigurable Processor for Heterogeneous Multi-core Architectures ,2015   **Low-cost Heterogeneous Embedded Multiprocessor Architecture for Real-time Stream Processing Applications** Berend Hendrik Jan Dekens,2015   **Chip Multiprocessor Generator** Ofer Shacham,2011 Recent changes in technology scaling have made power dissipation today s major performance limiter As a result designers struggle to meet performance requirements under stringent power budgets At the same time the traditional solution to power efficiency application specific designs has become prohibitively expensive due to increasing nonrecurring engineering NRE costs Most concerning are the development costs for design validation and software for new systems In this thesis we argue that one can harness ideas of reconfigurable designs to build a design framework that can generate semi custom chips a Chip Generator A domain specific chip generator codifies the designer knowledge and design trade offs into a template that can be used to create many different chips Like reconfigurable designs these systems fix the top level system architecture amortizing software and validation and design costs and enabling a rich system simulation environment for application developers Meanwhile below the top level the developer can program the individual inner components of the architecture Unlike reconfigurable chips a generator compiles the program to create a customized chip This compilation process occurs at elaboration time long before silicon is fabricated The result is a framework that enables

more customization of the generated chip at the architectural level because additional components and logic can be added if the customization process requires it At the same time this framework does not introduce inefficiency at the circuit level because unneeded circuit overheads are not taped out Using Chip Generators we argue will enable design houses to design a wide family of chips using a cost structure similar to that of designing a single chip potentially saving tens of millions of dollars while enabling per application customization and optimization   *Reconfigurable and Adaptive Computing* Nadia Nedjah,Chao Wang,2018-10-09 Reconfigurable computing techniques and adaptive systems are some of the most promising architectures for microprocessors Reconfigurable and Adaptive Computing Theory and Applications explores the latest research activities on hardware architecture for reconfigurable and adaptive computing systems The first section of the book covers reconfigurable systems The book presents a software and hardware codesign flow for coarse grained systems on chip a video watermarking algorithm for the H 264 standard a solution for regular expressions matching systems and a novel field programmable gate array FPGA based acceleration solution with MapReduce framework on multiple hardware accelerators The second section discusses network on chip including an implementation of a multiprocessor system on chip platform with shared memory access end to end quality of service metrics modeling based on a multi application environment in network on chip and a 3D ant colony routing 3D ACR for network on chip with three different 3D topologies The final section addresses the methodology of system codesign The book introduces a new software hardware codesign flow for embedded systems that models both processors and intellectual property cores as services It also proposes an efficient algorithm for dependent task software hardware codesign with the greedy partitioning and insert scheduling method GPISM by task graph   *Reconfigurable Computing for Real-time Applications* Peter John Waldeck,2005   *Towards Heterogeneous Multi-core Systems-on-Chip for Edge Machine Learning* Vikram Jain,Marian Verhelst,2023-09-15 This book explores and motivates the need for building homogeneous and heterogeneous multi core systems for machine learning to enable flexibility and energy efficiency Coverage focuses on a key aspect of the challenges of extreme edge computing i e design of energy efficient and flexible hardware architectures and hardware software co optimization strategies to enable early design space exploration of hardware architectures The authors investigate possible design solutions for building single core specialized hardware accelerators for machine learning and motivates the need for building homogeneous and heterogeneous multi core systems to enable flexibility and energy efficiency The advantages of scaling to heterogeneous multi core systems are shown through the implementation of multiple test chips and architectural optimizations   **Reconfigurable Multithreaded Processors for Programmable Communication Systems** Suman Mamidi,2007   **Reconfigurable Computing** Maya B. Gokhale,Paul S. Graham,2006-07-04 A one of a kind survey of the field of Reconfigurable Computing Gives a comprehensive introduction to a discipline that offers a 10X 100X acceleration of algorithms over microprocessors Discusses the impact of reconfigurable hardware on a wide range of applications signal and image processing network security bioinformatics and

supercomputing Includes the history of the field as well as recent advances Includes an extensive bibliography of primary sources *Reconfigurable Computing: Architectures, Tools and Applications* Philip Brisk,José Gabriel de Figueiredo Coutinho,Pedro Diniz,2013-03-12 This book constitutes the thoroughly refereed conference proceedings of the 9th International Symposium on Reconfigurable Computing Architectures Tools and Applications ARC 2013 held in Los Angeles CA USA in March 2013 The 28 revised papers presented consisting of 20 full papers and 11 poster papers were carefully selected from 41 submissions The topics covered are applications arithmetic design optimization for FPGAs architectures place and routing Reconfigurable Computing Scott Hauck,André DeHon,2010-07-26 Reconfigurable Computing marks a revolutionary and hot topic that bridges the gap between the separate worlds of hardware and software design the key feature of reconfigurable computing is its groundbreaking ability to perform computations in hardware to increase performance while retaining the flexibility of a software solution Reconfigurable computers serve as affordable fast and accurate tools for developing designs ranging from single chip architectures to multi chip and embedded systems Scott Hauck and Andre DeHon have assembled a group of the key experts in the fields of both hardware and software computing to provide an introduction to the entire range of issues relating to reconfigurable computing FPGAs field programmable gate arrays act as the computing vehicles to implement this powerful technology Readers will be guided into adopting a completely new way of handling existing design concerns and be able to make use of the vast opportunities possible with reconfigurable logic in this rapidly evolving field Designed for both hardware and software programmers Views of reconfigurable programming beyond standard programming languages Broad set of case studies demonstrating how to use FPGAs in novel and efficient ways *Assigning Real-time Tasks to Heterogeneous Processors by Applying Ant Colony Optimization* Hua Chen,2005 Run-Time Reconfigurable Instruction Set Processor Muhammad Aqeel Iqbal,Shoab Ahmed Khan,2012 Run Time Reconfigurable Instruction Set Processors are next generation processors which can optimize their instruction sets according to the demands of the applications being under execution on them This optimization is achieved through reconfiguration in their hardware on fly In this way the reconfigurable processors adapt their hardware which is most suitable one for the running application and consequently they enhance the performance Reconfigurable instruction set processors are the programmable processors that contain the reconfigurable logic in one or more of their functional units The hardware design of such type of processors can be categorized into two main tasks The design of reconfigurable logic itself and the design of the communication interface of reconfigurable logic with the remaining modules of the processor

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